What is claimed is:

1. A charge transfer device comprising a charge transfer section for transferring information charges in packet units, an output section provided on the output side of said charge transfer section for converting, in packet units, said information charges into a voltage signal, and a source follower amplification circuit for extracting a voltage signal subjected to impedance conversion obtained by said output section,

wherein said source follower amplification circuit comprises:

an amplification transistor which receives, at a gate, the voltage signal from said output section and outputs, from a source, an output signal corresponding to a change in the voltage signal;

a load transistor connected between said amplification transistor and a first power source for causing a constant current to flow from said amplification transistor to the side of the first power source; and

a control transistor connected between said amplification transistor and a second power source, wherein said control transistor cuts off a current flowing from the second power source to said amplification transistor according to a control signal.

2. A charge transfer device according to claim 1, wherein said device comprises an input terminal which is connected to a gate of said control transistor and to a gate of said load transistor commonly.

3. A charge transfer device according to claim 2, wherein said device comprises a control signal generating circuit provided between the gate of said control transistor and said input terminal for generating said control signal based on an input signal externally input to said input terminal, and said load transistor maintains an on state with regard to said input signal.

4. A charge transfer device according to claim 1, wherein said control transistor is of an enhancement type.

5. A charge transfer device according to claim 4, wherein said device comprises an input terminal which is connected to a gate of said control transistor and to a gate of said load transistor commonly.

6. A charge transfer device according to claim 5, wherein said device comprises a control signal generating circuit provided between the gate of said control transistor and said input terminal for generating said control signal based on an input signal externally input to said input

terminal, and said load transistor maintains an on state with regard to said input signal.